

Electronic Acknowledgement Receipt

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Title of Invention:	Techniques for grouping circuit elements into logic blocks
First Named Inventor/Applicant Name:	Ketan Padalia
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)	Multi Part /.zip	Pages (if appl.)
1		Suppl_AMD_015114-069200 US_070504.pdf	121446	yes	8

	Multipart Description/PDF files in .zip description		
	Document Description	Start	End
	Supplemental Response or Supplemental Amendment	1	1
	Claims	2	7
	Applicant Arguments/Remarks Made in an Amendment	8	8

Warnings:

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If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

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